REMARKS

The following is in response to the Office Communication mailed on August 17, 2004, which required information related to the declaration of an interference and support for the pending claims. As noted in the Communication, claims 40-57 are respectively exact copies of claims 1-18 of U.S. patent number 6,538,926, of Kato *et al.* issued March 25, 2003. The present Response cancels claims 41-46 and 52 and changes the dependence of claim 53. A two-column listing of the pending claims that applies each limitation or element of the pending claims to the disclosure of the application is given below. This is followed by a Request for Declaration of Interference, which is believed to provide the requested information.

SUPPORT FOR PENDING CLAIMS

The pending claims of present application, including the proposed Count 1, are primarily concerned with the "Serial Protocol and Device" and "Controller Module" aspects of the present invention, primarily described in paragraphs [0072] and [0111] although additional details are provided in other sections. Particular attention is called to paragraphs [0095]-[0111].

The present application provides a number of differing embodiments and has a number of elements that can be taken as the "buffer memory" of the claims, such as elements 219 (Fig. 4), 337 (Fig. 6A), 413 (Fig. 7A), or 607 (Fig. 8B). Independent claims 40 and 51 differ from each other in that the first of these only has "a buffer memory", while claim 51 recites a plurality of nonvolatile memories *each* including a buffer memory. Although other embodiments are possible that recite a buffer memory, but not one for each of a plurality of memories, the same element (337) is referred to in the support for both of these independent claims.

References are to the clean version of the Substitute Specification submitted concurrently with the filing of the present application.

40. A nonvolatile memory system comprising:	Memory system: 129 of Figs. 1A, 1B.
a nonvolatile memory including a	Each memory module 131 contains one or more devices 141 [Figs. 2A, 2B] with cell array 201 [Fig. 4]. In one embodiment,

plurality of nonvolatile memory cells and a buffer memory; and a control device coupled to said nonvolatile memory,	element 337 [Fig. 6A] can be taken as the buffer.
wherein said control device is enabled to receive data from outside of said nonvolatile memory system and to apply said data to said nonvolatile memory,	Controller: 133/134 of Fig. 1A/1B. Figs. 1A, 1B., controller 133, 134 connected to outside of memory system along bus 123, 138.
wherein said nonvolatile memory is enabled to operate a program operation,	¶[0106]: "The microprocessor 121 then writes the R/W state machine 613 with a vector for a write command. The R/W state machine 613 selects the address registers 605 as the data source and enables the protocol state machine 623 to begin. ..."
wherein in said program operation, said nonvolatile memory receives said data from said control device, stores said data to said buffer memory and stores said data in said buffer memory to ones of said nonvolatile memory cells,	¶[0081], lns. 5-6: "the information from the serial lines SI0, SI1 are now shifted into the enabled data shift register 337 and interpreted as data." ¶[0075], lns. 5-6: "the data shift register 337 shifts in a 64-bit chunk of data, and outputs it in parallel on a WRITE data bus 347."
wherein said control device is enabled to receive data from outside of said nonvolatile memory system, while said nonvolatile memory is operating in said program operation, and	¶[0107]: "As data is shifted to the memory device the system microprocessor 121 [Fig. 1] continues to load data into the SERDES serial-parallel converter 607 [Fig. 8B] keeping data ready to be shifted to the memory device. ..."
wherein said buffer memory has a data storing capacity enabling the receiving of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation, said data length being more	In the terminology of the application, a chunk is unit of data stored in a program operation: "In the preferred embodiment, dta is written and read in a 64-bit chunk." [¶[0093], ln.1]

than 1 byte.	¶[0075], lns. 5-6: "the data shift register 337 shifts in a 64-bit chunk of data, and outputs it in parallel on a WRITE data bus 347."

The present application describes the structure of Flash EEPROM memory devices at paragraphs [0056]-[0058]. Many of the details are not explicitly recited in the present application, but are instead to be found in U.S. patents 5,172,338 and 5,297,148. Paragraph [0057] explicitly incorporates these patents by reference into the present application and, as such, they form an integral part of the present application.

47. A nonvolatile memory system according to claim 40, wherein said nonvolatile memory includes a plurality of word lines and a plurality of data lines, and wherein each of said nonvolatile memory cells is arranged at a crossing point of a corresponding one of said word lines and a corresponding one of said data lines and is coupled to the corresponding word line and corresponding data line.	See 141 Fig. 4, for an exemplary memory device including cell array 201. For the structure in terms of word lines and data lines, see, for example, U.S. patent 5,172,338, Fig. 4.
48. A nonvolatile memory system according to claim 47, wherein said nonvolatile memory includes a plurality of sectors each comprising one word line and ones of the nonvolatile memory cells coupled thereto, and wherein said buffer memory has a data storing capacity enabling the receiving of a unit of data of a length equal to the data storing capacity and enabling the storing of a unit of data in said	On the structure of the memory (sectors, wordlines, cells), again see U.S. patent 5,172,338, especially beginning at col. 19, line 10. For the storing capacity of the buffer memory, see ¶[0075], lns. 5-6: "the data shift register 337 shifts in a 64-bit chunk of data, and outputs it in parallel on a WRITE data bus 347."

sector.

49. A nonvolatile memory system according to claim 48, wherein said nonvolatile memory is a flash memory.	¶[0057]: "In the preferred embodiment, an array of flash electrically-erasable-programmable-read-only memories (EEPROM's) in the form of an integrated circuit chip is employed as the memory device 141. ..."
50. A nonvolatile memory system according to claim 40, wherein said control device includes a host interface comprised of a data bus transceiver, an address bus driver, an address decoder and a control bus controller, to enable communication between the nonvolatile memory and an external system bus.	The control device can be taken as 133 (or 133 and 137) of Fig. 1A, with detail shown in Figs. 7A and 8A, or 134 of Fig. 1B, with detail shown in Figs. 7B and 8B. In the first case, the recited elements can be taken as elements 411, 415, 417, 511, 543, 533. In the second case, elements 601, 605, 607, 611, 613, 615. The external system bus is123 (or 138).
51. A nonvolatile memory system comprising: a plurality of nonvolatile memories each including a plurality of nonvolatile memory cells and a buffer memory; and a control device coupled to said nonvolatile memories, wherein said control device is enabled to receive data from outside of said nonvolatile memory system and to apply said data to said nonvolatile memories, wherein said nonvolatile memories are enabled to operate a program operation,	Memory system: 129 of Figs. 1A, 1B. Each memory module 131 contains one or more devices 141 [Figs. 2A, 2B] with cell array 201 [Fig. 4]. In one embodiment, element 337 [Fig. 6A] can be taken as the buffer. Controller: 133/134 of Fig. 1A/1B. Figs. 1A, 1B., controller 133, 134 connected to outside of memory system along bus 123, 138. ¶[0106]: "The microprocessor 121 then writes the R/W state machine 613 with a

vector for a write command. The R/W state machine 613 selects the address registers 605 as the data source and enables the protocol state machine 623 to begin. ..."

wherein in said program operation, each of said nonvolatile memories selectively receives said data from said control device, stores said data to said buffer memory thereof and stores said data in said buffer memory to ones of said nonvolatile memory cells of that nonvolatile memory,

¶[0081], lns. 5-6: "the information from the serial lines SI0, SI1 are now shifted into the enabled data shift register 337 and interpreted as data."

¶[0075], lns. 5-6: "the data shift register 337 shifts in a 64-bit chunk of data, and outputs it in parallel on a WRITE data bus 347."

wherein said control device is enabled to receive data from outside of said nonvolatile memory system, while said nonvolatile memories are operating in said program operation, and

¶[0107]: "As data is shifted to the memory device the system microprocessor 121 [Fig. 1] continues to load data into the SERDES serial-parallel converter 607 [Fig. 8B] keeping data ready to be shifted to the memory device. ..."

wherein said buffer memory has a data storing capacity enabling the receiving of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation, said data length being more than 1 byte.

In the terminology of the application, a chunk is unit of data stored in a program operation: "In the preferred embodiment, dta is written and read in a 64-bit chunk." [¶[0093], ln.1]

¶[0075], lns. 5-6: "the data shift register 337 shifts in a 64-bit chunk of data, and outputs it in parallel on a WRITE data bus 347."

53. A nonvolatile memory system according to claim 51,

wherein each of said nonvolatile memories further includes a plurality of word

See 141 Fig. 4, for an exemplary memory device including cell array 201. For the structure in terms of word lines and data lines, see, for example, U.S. patent 5,172,338,

lines and a plurality of data lines, and wherein each of said nonvolatile memory cells in each of the nonvolatile memories is arranged at a crossing point of a corresponding one of said word lines and a corresponding one of said data lines and is coupled to said corresponding word line and corresponding data line.	Fig. 4.
54. A nonvolatile memory system according to claim 53, wherein each of said nonvolatile memories includes a plurality of sectors each comprising one word line and ones of the nonvolatile memory cells coupled thereto, and wherein said buffer memory has a data storing capacity for receiving data in units of a sector and enabling the storing of a unit of data in said sector.	On the structure of the memory (sectors, wordlines, cells), again see U.S. patent 5,172,338, especially beginning at col. 19, line 10. For the storing capacity of the buffer memory, see ¶[0075], lns. 5-6: "the data shift register 337 shifts in a 64-bit chunk of data, and outputs it in parallel on a WRITE data bus 347."
55. A nonvolatile memory system accordance to claim 54, wherein each of said nonvolatile memories is a flash memory.	¶[0057]: "In the preferred embodiment, an array of flash electrically-erasable-programmable-read-only memories (EEPROM's) in the form of an integrated circuit chip is employed as the memory device 141. ..."
56. A nonvolatile memory system according to claim 55, wherein said control device includes a host interface comprised of a data bus	The control device can be taken as 133 (or 133 and 137) of Fig. 1A, with detail shown in Figs. 7A and 8A, or 134 of Fig. 1B, with detail shown in Figs. 7B and 8B. In the

transceiver, an address bus driver, an address decoder and a control bus controller, to enable communication between the nonvolatile memories and an external system bus.

first case, the recited elements can be taken as elements 411, 415, 417, 511, 543, 533. In the second case, elements 601, 605, 607, 611, 613, 615. The external system bus is123 (or 138).

57. A nonvolatile memory system according to claim 51,

wherein said control device includes a host interface comprised of a data bus transceiver, an address bus driver, an address decoder and a control bus controller, to enable communication between the. nonvolatile memories and an external system bus.

The control device can be taken as 133 (or 133 and 137) of Fig. 1A, with detail shown in Figs. 7A and 8A, or 134 of Fig. 1B, with detail shown in Figs. 7B and 8B. In the first case, the recited elements can be taken as elements 411, 415, 417, 511, 543, 533. In the second case, elements 601, 605, 607, 611, 613, 615. The external system bus is123 (or 138).

REQUEST FOR DECLARATION OF INTERFERENCE

It is respectfully requested that an interference be declared between the present application and U.S. patent number number 6,538,926, of Kato *et al.*, referred to below as the "'926 patent". Claims 40 and 47-51 are respectively exact copies of claims 1 and 8-12 of U.S. patent number 6,538,926, of Kato *et al.* issued March 25, 2003, and claims 53-57 are closely modeled on claims 14-18 of '926 patent (the dependence of claim 53 has been changed). Claim 40 of the present application, which is an exact copy of claim 1 of the '926 patent, is suggested as a first count for the interference, as follows:

Count 1

A nonvolatile memory system comprising:

a nonvolatile memory including a plurality of nonvolatile

memory cells and a buffer memory; and a control device coupled to said nonvolatile memory, wherein said control device is enabled to receive data from outside of said nonvolatile memory system and to apply said data to said nonvolatile memory,

wherein said nonvolatile memory is enabled to operate a program operation,

wherein in said program operation, said nonvolatile memory receives said data from said control device, stores said data to said buffer memory and stores said data in said buffer memory to ones of said nonvolatile memory cells,

wherein said control device is enabled to receive data from outside of said nonvolatile memory system, while said nonvolatile memory is operating in said program operation, and

wherein said buffer memory has a data storing capacity enabling the receiving of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation, said data length being more than 1 byte.

35 U.S.C. 135(b)

Claim 40 of the present application was added by Preliminary Amendment, simultaneously with the filing of the present application on March 24, 2004. This is less than one year after the '926 patent was granted on March 25, 2003.

Effective Filing Date

As specified in the "Cross-Reference to Related Application" section, as amended by the Preliminary Amendment filed concurrently with the present application, of paragraph [0001] of the application, the present application is a continuation entitled to an effective filing date of July 26, 1991 due to the benefit of:

U.S. Application Serial No. 10/785,373, filed on February 23, 2004,

U.S. Application Serial No. 09/939,290, filed on August 22, 2001,

U.S. Application Serial No. 09/657,369, filed on September 8, 2000, now Patent No. 6,317,812,

U.S. Application Serial No. 09/064,528, filed on April 21, 1998, now Patent No. 6,148,363,

U.S. Application Serial No. 08/931,193, filed on September 16, 1997, now Patent No. 5,806,070,

U.S. Application Serial No. 08/396,488, filed on March 2, 1995,

U.S. Application Serial No. 07/736,733, filed on July 26, 1991, now Patent No. 5,430,859.

The `926 patent is shown to have a United States filing date of October 31, 2001, claiming priority from a series of continuations and divisions back to U.S. Application Serial No. 08/164,780, filed on December 10, 1993, now Patent No. 5,592,415, which is a continuation-in-part of abandoned U.S. Application Serial No. 08/085,156, filed on July 2, 1993, and claims priority from a Japanese application filed July 6, 1992. The earliest of these U.S. applications is well over a year later than the July 26, 1991, effective filing date of the present application, with the Japanese application just under a year later than the July 26, 1991, effective filing date of the present application.

Therefore, it is requested that the interference be declared with the Applicants of the present application designated the senior party.

Claims Corresponding to the Proposed Count 1

The proposed Count 1 is an exact copy of claim 1 of the `926 patent. Claims 8-11 of the `926 patent are dependent on claim 1. Claim 12 of the `926 patent is an independent claim that differs from claim1 in that it recites a plurality of nonvolatile memories *each* including a buffer memory. Claims 14-18 of the `926 patent are dependent claims.

Support for the Proposed Count 1 in the Present Application

The pending claims of present application, including the proposed Count 1, are primarily concerned with the "Serial Protocol and Device" and "Controller Module" aspects of the present invention, primarily described in paragraphs [0072] and [0111] although additional details are provided in other sections. Particular attention is called to paragraphs [0095]-[0111].

The present application provides a number of differing embodiments and has a number of elements that can be taken as the "buffer memory" of the claims, such as elements 219 (Fig. 4), 337 (Fig. 6A), 413 (Fig. 7A), or 607 (Fig. 8B). Independent claims 40 and 51 differ from each other in that the first of these only has "a buffer memory", while claim 51 recites a plurality of nonvolatile memories *each* including a buffer memory. Although other embodiments are possible that recite a buffer memory, but not one for each of a plurality of memories, the same element (337) is referred to in the support for both of these independent claims.

References are again to the clean version of the Substitute Specification submitted concurrently with the filing of the present application.

Count 1	Present Application
A nonvolatile memory system comprising:	Memory system: 129 of Figs. 1A, 1B.
a nonvolatile memory including a plurality of nonvolatile memory cells and a buffer memory; and a control device coupled to said nonvolatile memory,	Each memory module 131 contains one or more devices 141 [Figs. 2A, 2B] with cell array 201 [Fig. 4]. In one embodiment, element 337 [Fig. 6A] can be taken as the buffer.
	Controller: 133/134 of Fig. 1A/1B.
wherein said control device is enabled to receive data from outside of said nonvolatile memory system and to apply said data to said nonvolatile memory,	Figs. 1A, 1B., controller 133, 134 connected to outside of memory system along bus 123, 138.
wherein said nonvolatile memory is enabled to operate a program operation,	¶[0106]: "The microprocessor 121 then writes the R/W state machine 613 with a vector for a write command. The R/W state machine 613 selects the address registers 605

	as the data source and enables the protocol state machine 623 to begin. ..."
wherein in said program operation, said nonvolatile memory receives said data from said control device, stores said data to said buffer memory and stores said data in said buffer memory to ones of said nonvolatile memory cells,	¶[0081], lns. 5-6: "the information from the serial lines SI0, SI1 are now shifted into the enabled data shift register 337 and interpreted as data." ¶[0075], lns. 5-6: "the data shift register 337 shifts in a 64-bit chunk of data, and outputs it in parallel on a WRITE data bus 347."
wherein said control device is enabled to receive data from outside of said nonvolatile memory system, while said nonvolatile memory is operating in said program operation, and	¶[0107]: "As data is shifted to the memory device the system microprocessor 121 [Fig. 1] continues to load data into the SERDES serial-parallel converter 607 [Fig. 8B] keeping data ready to be shifted to the memory device. ..."
wherein said buffer memory has a data storing capacity enabling the receiving of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation, said data length being more than 1 byte.	In the terminology of the application, a chunk is unit of data stored in a program operation: "In the preferred embodiment, dta is written and read in a 64-bit chunk." [¶[0093], ln.1] ¶[0075], lns. 5-6: "the data shift register 337 shifts in a 64-bit chunk of data, and outputs it in parallel on a WRITE data bus 347."

For these reasons, it is submitted to be clear that claim 1 of the `926 patent is supported by the present application disclosure, first filed on July 26, 1991.

'926 Patent Prosecution File History

A review of the file history of the '926 patent reveals that the material in the present application was not cited during the '926 patent application process, although a related patent (U.S. 5,663,901) was cited in an Information Disclosure Statement, but not otherwise discussed.

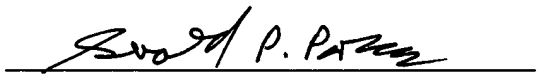
Information Disclosure Statement

An Information Disclosure Statement and accompanying forms 1449 are being prepared in order to cite references cited in the '926 patent and its parents and should be submitted within the next few weeks.

Conclusion

It is believed that the above provides the information required by the Communication. A prompt declaration of the requested interference is respectfully requested. In the meantime, however, if the Examiner has any questions about this request, application or disclosure statements, a telephone call to the undersigned is invited.

Respectfully submitted,



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